XP-002114028

ADDRESSING A SECOND PAGE OF REGISTERS WITHOUT INCREASING THE REGISTER FIELD LENGTH

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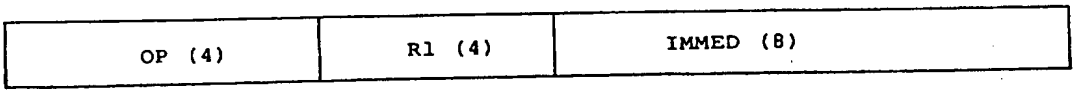
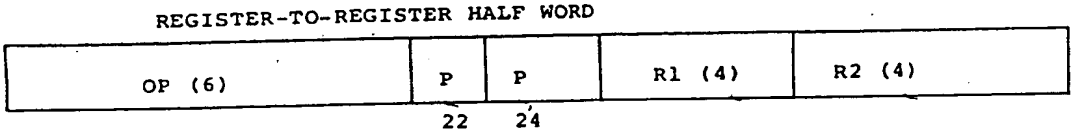
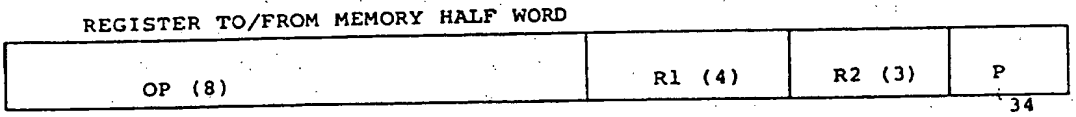
IMMEDIATE TO HALF-WORD REGISTER



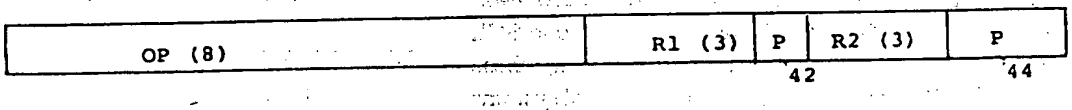
REGISTER-TO-REGISTER HALF WORD



REGISTER TO/FROM MEMORY HALF WORD



FULL-WORD REGISTER-TO-REGISTER



The described second page addressing concept is particularly useful in a computer having the following design constraints:

1) Maximum instruction lengths of 16 bits;
2) An immediate field of not less than eight bits;
3) A memory word size of 16 bits;
4) More than eight full-word registers addressable at eight-bit byte boundaries; and
5) The length and location of all instruction fields selected so as not to cross eight-bit boundaries.

Two separate pages of registers, each containing eight full-word registers, and each page being located anywhere in a plural page register storage can be addressed by the use of a page bit located in various unused bit positions, which become available within an instruction format as the result of the operation specified by the OP code. The page bit, or its absence which indicates the default page, points to a page pointer register, the contents of which identifies the page within which

operand registers are located.

To meet the above design constraints, immediate-to-register instructions require all bit positions without redundancy and, therefore, can only be performed using a single default page of registers. For half-word (eight bits) register-to-register operations, the eight-bit immediate field is not needed and therefore the remaining eight bits are available for other purposes. Inasmuch as the immediate OP code was only four bits, additional instructions operating on registers located either in a default page or in a second page can be specified, using two additional OP code modifier bits yielding a total OP code field of six bits. The two remaining bit positions labeled 22 and 24 can then be used to select either a default or a second page pointer register, the contents of which identify the page within which registers R1 or R2 are located, respectively. For example, a 0 bit could indicate the default page pointer register and a 1 bit could indicate the second page pointer register.

When executing instructions involving a full word such as instructions involving a memory address which is a full 16-bit word, or when executing full-word register-to-register instructions, only even numbered registers need be addressed. This is so because two half-word registers are required to store a full word, and the even numbered register of a pair of registers, therefore, specifies both registers completely. This allows use of the lower order bit positions of the register specification field as the page identification bit, leaving a full eight bits available for use as OP codes. For example, the half-word register-to-memory store instruction requires a four-bit R1 field, in order to completely specify the address within a default page of the half-word register which contains the eight-bits to be stored.

On the other hand, only a three-bit field is needed to specify both even and odd registers containing the 16-bit memory address, to which the contents of R1 is to be stored. Thus the lowest order bit position 34 of the R2 field is redundant when used with these OP codes and, therefore, is available to select a default or a second page pointer register, the contents of which identify the page within which register R2 is located.

When a full-word register-to-register instruction is to be executed, only three bits are needed to completely specify the starting address of full-word register pair R1 and full-word register pair R2. This leaves lower order bit position 42 of register R1 specification field and lower order bit position 44 of register R2 specification field available, for use with these particular OP codes as default/second page designation bits, thereby allowing execution of instructions between registers in different pages. For example, a full-word register-to-register addition could be performed between register 1 of either a default page or a second page, and register 2 of either a default page or a second page.